REMARKS

Claims 1-49 are currently pending in the application. Claims 1-49 were rejected in the Final Office Action mailed on April 4, 2007. Claims 1, 22, 27, 28, 44, and 49 have been amended. Claims 23-26 and 45-48 have been canceled.

The Examiner objected to the form of claims 22 and 44 as being ambiguous. Both claims have been amended to be in independent form. The objection is believed addressed thereby.

The Examiner maintained the rejection of claims 23-26 and 45-48 under 35 U.S.C. 112, first paragraph as failing to comply with the enablement requirement. The traversal of this rejection in the previous response is maintained and incorporated herein by reference. However, notwithstanding the foregoing, claims 23-26 and 45-48 have been canceled in the interests of moving prosecution of the application forward. As these canceled claims are believed to be enabled by the present application as filed, the cancellation is not proposed for any reason related to patentability. The Applicants hereby reserve the right to pursue these canceled claims in this or subsequent related applications.

The Examiner maintained the rejection claims 1-14, 20, 22, 27-32, 34, 35, 37-42, 44, and 49 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,488,729 (Vegesna). The Examiner also maintained the rejection of claims 15-19, 33, 36, 43, and 45-48 under 35 U.S.C. 103(a) as being unpatentable over Vegesna in view of a variety of other references. The rejections have been traversed in previous responses and those arguments are maintained and incorporated herein by reference.

The claims of the present application are clearly distinguishable from the system described in Vegesna which employs conventional synchronous techniques and, as discussed in the previous response, repeatedly stresses that a key aspect of its approach is that the instructions issued to its parallel pipelines are issued, i.e., enter the pipelines, *simultaneously*. See, for example, column 1, lines 16-22; column 2, lines 56-61 and 64-67; column 3, lines 11-13; column

14, lines 59-61; column 23, lines 8-11; column 29, lines 34-37; etc. Indeed, because Vesegna's architecture is controlled by a clock signal, units of data can only be issued to its pipelines on a clock transition, and can therefore only be issued to the pipelines simultaneously. See for example, the various figures relating units of data to clock cycles.

Moreover, claim 1 recites that "the asynchronous circuit is operable to *sequentially control* transmission of the units of data in the pipelines." As discussed above, Vesegna does not employ sequential control of data transmission in its pipelines. Rather, it relies on a clock signal which synchronizes simultaneous transmission of data across the parallel pipelines.

As discussed in the present application, the approach recited in the claims of the present application has significant benefits over parallel pipelines implemented using conventional synchronous design techniques. That is, synchronous parallel pipelines process parallel data units simultaneously and therefore must determine any dependencies between the data units and, if any are found, manipulate the flow of one or both pipelines to handle the dependency. This is extremely expensive in chip resources and severely limits the scale and efficiency of N-way synchronous pipelines. On the other hand, because the pipelines of the present invention are not synchronized with each other, i.e., their operation is staggered in time, the units of data, while in parallel pipelines, are effectively processed sequentially. So, if there is a logical dependency, the asynchronous nature of the pipelines can be leveraged to hold the affected pipeline(s) using far simpler mechanisms. Thus, embodiments of the present invention enjoy the benefits of multiple-issue architectures with some of the simplicity of a single-issue architecture. See, for example, paragraphs [0022]-[0024] of the present application.

In view of the fact that Vesegna's architecture is a synchronous architecture which requires the simultaneous issuance of instructions to its pipelines, and does not employ sequential control of its pipelines, the rejection of claims 1, 22, 27, 28, 44, and 49 is believed overcome. In addition, the rejection of claim 2-21 and 29-43 is believed overcome for at least

the reasons discussed.

Notwithstanding the foregoing, claims 1, 22, 27, 28, 44, and 49 have been amended to more clearly describe the invention. More specifically, these claims have been amended to recite that the asynchronous circuit or the N-way issue resource is "configured to employ asynchronous flow control…characterized by an average cycle time," and that the data units are issued to the respective pipelines "staggered in time such that up to N data units enter the N pipelines during the average cycle time." These amendments are supported in the present specification, for example, at paragraphs [0017]-[0023].

As discussed above, the foregoing amendments are not believed necessary to distinguish the claimed invention from the art of record, and are being proposed for clarification purposes only, and not for any reason related to patentability. And in view of the fact that none of the art of record teaches or suggests the recited combination of features, it is respectfully requested that the rejections be withdrawn.

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (510) 663-1100.

Respectfully submitted,
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